AMENDMENTS TO THE CLAIMS

This listing of the claims will replace all prior versions and listings of claims in the application:

Listing of Claims

1. (currently amended) A method of equalizing voltage transitions of a pair of differential signals, said method comprising:

generating a signal to cause a capacitance to be conductively coupled to two circuit nodes, said capacitance operative to boost the transition speed of said differential signals and comprising two series-connected capacitive elements;

receiving said differential signals, one of said signals being at higher voltage than the other of said signals; and

boosting the transition speed of said differential signals with said conductively coupled capacitance.

2. (currently amended) The method of claim 1 wherein said generating comprises generating a signal to cause an integrated circuit capacitor to be conductively coupled between two circuit nodes, said capacitor operative to boost the transition speed of said differential signals and connected in series to another capacitive element.

3. (currently amended) ~~The~~ A method of ~~claim 1 wherein said generating comprises~~ equalizing voltage

transitions of a pair of differential signals, said method comprising:

generating a signal to cause two integrated circuit varactors to be conductively coupled between two circuit nodes, said two varactors coupled in series to each other and operative to boost the transition speed of said differential signals;

receiving said differential signals, one of said signals being at higher voltage than the other of said signals; and

boosting the transition speed of said differential signals with said conductively coupled varactors.

4. (currently amended) A method of equalizing voltage transitions of a pair of differential signals, said method comprising:

providing a first selectable capacitance operative to boost the transition speed of said differential signals, said first selectable capacitance comprising serially connected integrated circuit capacitive elements; and

providing a second selectable capacitance operative to boost the transition speed of said differential signals either alone or in combination with said first selectable capacitance.

5. (original) The method of claim 4 further comprising providing a third selectable capacitance operative to boost the transition speed of said differential signals either alone, in combination with said first selectable capacitance, in combination with said second selectable capacitance, or in combination with said first and said second selectable capacitances.

6. (original) The method of claim 4 wherein said first and second selectable capacitances are coupled in parallel with respect to each other.

7. (original) The method of claim 4 wherein said first selectable capacitance comprises an integrated circuit capacitor.

8. (currently amended) ~~The~~ A method of ~~claim 4 wherein said first selectable capacitance comprises two~~ equalizing voltage transitions of a pair of differential signals, said method comprising:

providing a selectable pair of integrated circuit varactors coupled in series to each other and operative to boost the transition speed of said differential signals; and

providing a selectable capacitance operative to boost the transition speed of said differential signals either alone or in combination with said selectable pair.

9. (currently amended) ~~The~~ A method of ~~claim 4 wherein said first selectable capacitance comprises~~ equalizing voltage transitions of a pair of differential signals, said method comprising:

providing a selectable series connection of a first pass transistor, two integrated circuit capacitance devices, and a second pass transistor operative to boost the transition speed of said differential signals; and

providing a selectable capacitance operative to boost the transition speed of said differential signals either

alone or in combination with said selectable series connection.

10. (currently amended) A method of equalizing voltage transitions of a pair of differential signals, said method comprising:

generating a first signal to cause a first capacitance of two series-connected capacitive elements to be conductively coupled to circuitry operative to receive differential signals, said first capacitance operative to boost the transition speed of said differential signals; and

generating a second signal to cause a second capacitance to be conductively coupled to said circuitry operative to receive differential signals, said second capacitance operative to boost the transition speed of said differential signals either alone or in combination with said first capacitance.

11. (original) A method of equalizing voltage transitions of a pair of differential signals, said method comprising:

integrating a first series connection of a first pass transistor, two integrated circuit capacitance devices, and a second pass transistor between two nodes in an integrated equalization circuit operative to receive differential signals, said first series connection operative to boost the transition speed of said differential signals; and

integrating a second series connection of a first pass transistor, two integrated circuit capacitance devices, and a second pass transistor between said two nodes in said equalization circuit, said first and second series

connections being in parallel with respect to each other, said second series connection operative to boost the transition speed of said differential signals alone or in combination with said first series connection.

12. (currently amended) Equalization circuitry comprising:

a first node ~~at which a current flow transition from low current to high current occurs in response to a voltage transition of a first signal~~;

a second node ~~at which a current flow transition from high current to low current occurs in response to a transition of a second signal voltage~~;

a first series connection of a first switch, a first capacitance, a second capacitance, and a second switch coupled in series between said first and second nodes, said first and second switches opening substantially simultaneously and closing substantially simultaneously; and

a second series connection of a first switch, a capacitance, and a second switch coupled in series between said first and second nodes, said second series first and second switches opening substantially simultaneously and closing substantially simultaneously; wherein

said first and second series connections are coupled in parallel with respect to each other between said first and second nodes.

13. (currently amended) The equalization circuitry of claim 12 wherein each said capacitance of said first and second series connections comprises ~~devices~~ a device selected from the group consisting of capacitors and varactors.

14. (original) The equalization circuitry of claim 12 wherein at least one of said first and second switches of said first and second series connections comprises an N-channel MOSFET having a source, a drain, and a gate, said source or drain coupled to one of said nodes and the other of said source or drain coupled to one of said capacitances.

15. (original) A printed circuit board comprising said equalization circuitry of claim 12 mounted on said printed circuit board.

16. (original) The printed circuit board of claim 15 further comprising a memory mounted on said printed circuit board.

17. (original) The printed circuit board of claim 15 further comprising processing circuitry mounted on said printed circuit board.

18. (original) A digital processing system comprising:

a processor;

a memory coupled to said processor; and

said equalization circuitry of claim 12 coupled to at least one of said processor and said memory.

19. (currently amended) A digital processing system comprising:

a processor; and

a memory coupled to said processor, wherein at least one of said processor and said memory comprises ~~said~~ equalization circuitry ~~of claim 12~~ comprising:

a first node at which a current-flow transition from low current to high current occurs in response to a voltage transition of a first signal;

a second node at which a current-flow transition from high current to low current occurs in response to a transition of a second signal voltage;

a first series connection of a first switch, a capacitance, and a second switch coupled in series between said first and second nodes, said first and second switches opening substantially simultaneously and closing substantially simultaneously; and

a second series connection of a first switch, a capacitance, and a second switch coupled in series between said first and second nodes, said second series first and second switches opening substantially simultaneously and closing substantially simultaneously; wherein

said first and second series connections are coupled in parallel with respect to each other between said first and second nodes.

20. (original) Equalization circuitry comprising:

a first node at which a current-flow transition from low current to high current occurs;

a second node at which a current-flow transition from high current to low current occurs substantially simultaneously as said transition at said first node;

a first integrated circuit capacitance device having first and second terminals;

a first integrated circuit switch coupled in series between said first node and said first terminal of said first capacitance device;

a second integrated circuit capacitance device having first and second terminals, said first terminal of said second capacitance device coupled to said second terminal of said first capacitance device; and

a second integrated circuit switch coupled in series between said second terminal of said second capacitance device and said second node, said first and second switches opening substantially simultaneously and closing substantially simultaneously.

21. (original) The equalization circuitry of claim 20 wherein said first and second capacitance devices each comprise a capacitor.

22. (original) The equalization circuitry of claim 20 wherein said first and second capacitance devices each comprise a varactor.

23. (original) The equalization circuitry of claim 20 wherein said first and second switches each comprise a transistor having two main terminals and a control terminal, one of said two main terminals is coupled to one of said nodes and the other of said two main terminals is coupled to one of said capacitance device terminals.

24. (original) The equalization circuitry of claim 23 wherein said first and second switches each comprises a MOSFET and said two main terminals are the source and drain and said control terminal is the gate.

25. (original) The equalization circuitry of claim 24 wherein each said MOSFET is an N-channel MOSFET.

26. (original) A differential buffer circuit comprising said equalization circuitry of claim 20.

27. (original) An integrated circuit chip comprising said equalization circuitry of claim 20.

28. (original) A programmable logic device comprising said equalization circuitry of claim 20.

29. (original) A printed circuit board comprising said equalization circuitry of claim 20 mounted on said printed circuit board.

30. (original) The printed circuit board of claim 29 further comprising a memory mounted on said printed circuit board.

31. (original) The printed circuit board of claim 29 further comprising processing circuitry mounted on said printed circuit board.

32. (original) A digital processing system comprising:

a processor;

a memory coupled to said processor; and

said equalization circuitry of claim 20 coupled to at least one of said processor and said memory.

33. (original) A digital processing system comprising:

a processor; and

a memory coupled to said processor, wherein:

at least one of said processor and said memory comprises said equalization circuitry of claim 20.

34. (original) An equalization circuit comprising:

a first resistor having first and second terminals, said first terminal operative to be coupled to a source of power voltage;

a first transistor having first and second main terminals and a control terminal, said first main terminal coupled to said second terminal of said first resistor, said control terminal operative to receive one of a pair of differential signals;

first current sinking circuitry coupled to said second main terminal and operative to be coupled to a source of voltage less than said power voltage;

a second resistor having first and second terminals, said first terminal operative to be coupled to said power voltage;

a second transistor having first and second main terminals and a control terminal, said first main terminal coupled to said second terminal of said second resistor, said control terminal operative to receive the other of said pair of differential signals;

second current sinking circuitry coupled to said second main terminal of said second transistor and operative to be coupled to said voltage less than said power voltage;

a third resistor coupled in series between said second main terminals of said first and second transistors; and

at least one series connection of a first pass transistor, two series-coupled capacitance devices, and a second pass transistor, said series connection coupled in series between said second main terminals of said first and second transistors, said first and second pass transistors each having a control terminal operative to receive substantially simultaneously a signal to cause said first and second pass transistors to provide a conductive path between said capacitance devices and said second main terminals.

35. (original) An integrated circuit comprising said equalization circuit of claim 34.

36. (original) A programmable logic device comprising said equalization circuit of claim 34.

37. (original) A printed circuit board comprising said equalization circuit of claim 34 mounted on said printed circuit board.

38. (original) The printed circuit board of claim 37 further comprising a memory mounted on said printed circuit board.

39. (original) The printed circuit board of claim 37 further comprising processing circuitry mounted on said printed circuit board.

40. (original) A digital processing system comprising:

a processor; and

a memory coupled to said processor, wherein:

at least one of said processor, said memory, or said system comprises said equalization circuit of claim 34.

41. (currently amended) An electrical circuit comprising:

means for receiving differential electrical signals, one of said differential signals being at a high voltage and the other of said differential signals being at a low voltage;

means for producing output signal transitions in response to transitions of said differential signals;

a pair of serially connected capacitance means for boosting the transition speed of said output signal transitions; and

means for selecting ~~the amount of~~ said capacitance means ~~with which~~ to boost said transition speed.

42. (new) A method of increasing voltage transitions of received signals, said method comprising:

coupling two series-connected capacitive elements in series between two circuit nodes at which voltage level transitions from high to low and low to high are substantially opposite each other; and

conducting current through said capacitive elements to increase the transition speed of said voltage level transitions.

43. (new) The method of claim 42 wherein said capacitive elements comprises capacitors.

44. (new) The method of claim 42 wherein said capacitive elements comprises varactors.

45. (new) The method of claim 42 wherein said coupling comprises:

driving a first transistor coupled between one of said nodes and one of said capacitive elements into conduction; and

driving a second transistor coupled between the other of said nodes and the other of said capacitive elements into conduction substantially simultaneously as said first transistor.

46. (new) The method of claim 42 further comprising:

coupling instead of or in addition to said two series-connected capacitive elements a second pair of series-connected capacitive elements in series between said two circuit nodes, said second pair coupled to said nodes in parallel with respect to said two series-connected capacitive elements; and

conducting current through said second pair of capacitive elements to increase the transition speed of said voltage level transitions.